generated by the syndrome calculator 5, and an error detector 7 which detects the presence or absence of an error in the data which has been subjected to error correction, or which checks to see that all errors have been corrected. The bus control unit 3, the buffer memory 4, the syndrome calculator 5, the error corrector 6, and the error detector 7 are connected with each other via a data bus 11.

A DMA command 12 is transmitted from the system control unit 1 to the DMA control unit 2 in order to provide instructions to execute DMA. (The drawing shows the signal line of the command 12 for the sake of convenience. This holds true for the other signals). A DMA request 13 is transmitted from the DMA control unit 2 to the bus control unit 3 in order to request DMA. A buffer memory access signal 14 is transmitted to execute the reading or writing of data from or to the buffer memory 4. A syndrome data supply signal 15 indicates the supply of data in the buffer memory 4 to the syndrome calculator 5. Syndrome 16 is the product in the syndrome calculator 5.

An access request signal 17 is transmitted from the error corrector 6 to the bus control unit 3 in order to request access to the buffer memory 4. An error corrector access signal 18 is transmitted to execute the reading or writing of data from or to the error corrector 6. An error correction completion signal 19 indicates that error correction is completed in the error corrector 6. An error detector data supply signal 20 indicates the supply of data from the buffer memory 4 to the error detector 7. An error detection signal 21 indicates whether or not an error has been detected by the error detector 7.

Figure 4 shows the procedure of horizontal error correction in one sector.

The procedure of horizontal error correction in one sector in the prior art error correction device will be described as follows with reference to Figures 3 and 4.

Step (a-1): the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 so as to provide instructions to transfer data equivalent to one code word×13 times from the buffer memory 4 to the syndrome calculator 5.

Step (a-2): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5.

Step (a-3): the bus control unit 3 puts the data bus 11 in commission, and outputs the buffer memory access signal 14 and the syndrome data supply signal 15 to the buffer memory 4 and the syndrome calculator 5, respectively, so as to execute the data transfer from the buffer memory 4 to the syndrome calculator 5.

Step (a-4): the syndrome calculator 5 performs error detection every transferred code word, and outputs the syndrome 16 to the error corrector 6 if there is an error.

Step (a-5): the error corrector 6 calculates the position and value of the error, based on the syndrome 16. In order to correct an error in data on the buffer memory 4, the error corrector 6 provides the bus control unit 3 with the access request signal 17, thereby requesting readout of the error-containing data.

Step (a-6): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 and the error corrector access signal 18 to the buffer memory 4 and the error corrector 6, respectively, reads error-containing data from the buffer memory 4, and supplies the data to the error corrector 6.

Step (a-7): after correcting the error in the data supplied, the error corrector 6 transmits the access request signal 17 to the bus control unit 3 again so as to request writing of the error-corrected data in the buffer memory 4.

Step (a-8): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector 6 and overwrites the data in the buffer memory 4. At the same time, the error corrector 6 transmits the correction completion signal 19 to the system control unit 1.

Step (a-9): in order to check to see that the corrected data contain no more error, the system control unit 1 transmits the DMA command 12 to the DMA control unit 2 so as to provide instructions to transfer the data from the buffer memory 4 to the error detector 7.

Step (a-10): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the error corrector 7.

Step (a-11): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 and the error detector data supply signal 20 to the buffer memory 4 and the error detector 7, respectively, so as to execute the data transfer from the buffer